

## INTEGRATED CIRCUIT MEMORY DEVICES

### Related Application

This application is a divisional of U.S. Application Serial No. 10/100,719, filed March 19, 2002, <sup>now Patent No. 6,709,915</sup> which claims priority from Korean Patent Application No. 2001-30772, filed on June 1, 2001, the contents of each of which are herein incorporated by reference in their entirety.

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### Field of the Invention

The present invention relates to an integrated circuit memory device and a method of fabricating the same, and more particularly, to an integrated circuit memory device which is capable of enhancing the capacitance of a capacitor without increasing the height of the capacitor and a method of fabricating the same.

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### Background of the Invention

As the integration density of integrated circuit devices, increases, the area occupied by a unit cell continues to decrease. Since the driving capability of integrated circuit devices, such as dynamic random access memories (DRAM), is strongly dependent on the capacitance of a capacitor, a variety of attempts for increasing the capacitance of a capacitor have been carried out, irrespective of the decrease of the area occupied by the capacitor. Accordingly, in order to increase the capacitance of a capacitor by increasing the effective area of the capacitor, capacitors have been formed to have a three-dimensional structure, such as a concave shape, a cylinder shape, a fin shape, or a box shape.

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Hereinafter, a method of fabricating a conventional integrated circuit memory device including a concave-shaped storage node electrode will be described with reference to FIGS. 1A through 1C. In FIGS. 1A through 1C, the drawings indicated by "X direction" are cross-sectional views of a semiconductor substrate taken along a direction parallel to word lines, and the drawings indicated by "Y direction" are cross-sectional views of a semiconductor substrate taken along a direction parallel to bit lines.

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Referring to FIG. 1A, word line structures 15 are formed on a semiconductor substrate 10, on which an isolation layer 11 is formed, by a well-known method.